REMARKS

Claims 1-20 are pending in the application.

Claims 1-20 have been rejected.

Claims 1, 3 and 14 have been amended as set forth herein, and Claim 21 has been added. Therefore, Claims 1-21 are currently pending.

Claim 1 has been amended to recite the feature of 'simulating said circuit to identify one or more of said functional elements that is a source of propagation of said unknown state'. Support for this amendment can be found, e.g., in paragraph [0036] of the specification and step le of Figure 3.

Claim 1 has been further amended to recite the feature of 'wherein said determining step is arranged to identify if a functional element which is a source of propagation of said unknown state is a hazard or a synchronizer.' Support for this amendment may be found, e.g., in original claim 11.

Dependent claims 3 and 14, which the Examiner has objected to as being dependent upon a rejected base claim, have been rewritten in independent form including all of the limitations of the base claim. The applicant submits that these claims are now allowable over the prior art.

New independent claim 21 has been added reciting a computer readable medium containing executable components for performing the method of claim 1. Basis for this claim can be found, e.g., on page 8, paragraph [00019] of the specification.

Claims 8 and 14 are also amended to accommodate the Examiner's objections, and these objections are believed to be moot.

CLAIM REJECTIONS -- 35 U.S.C. §103

Claims 1, 2, 7-13 and 15-20 were rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent 6,353,906 to *Smith, et al.*, hereinafter Smith). The applicant respectfully submits that this is not the case for the reasons that will be discussed below:

The present application relates to the verification of adequate synchronization of signals transmitted between different clock environments in digital circuits. In particular, the application describes a method of testing a model of a digital circuit that ensures that all signals that require synchronization may be identified by simulation of the model. Many modern electronic devices are designed such that different parts of the circuit are controlled using different clock frequencies that may be asynchronous. Such designs will include multiple signals that cross the boundaries between clock environments. If these signals are not adequately synchronized, then the circuit will develop errors.

Synchronizer circuits comprising a plurality of flip-flops are known in the art and are often included to ensure adequate synchronization. However, the use of these circuits relies on the designer to identify signals that constitute synchronization hazards in the circuit and implement a synchronizer for the receipt of each signal. For modem integrated circuits, which may contain many different clock environments with multiple signals being transmitted between them, it is difficult for the designer to be sure that all synchronization hazards have been identified. This may be further complicated by the present trend of reusing blocks of circuit designs when designing new circuits. A designer may be unfamiliar with the internal workings of the block of circuit being reused and it may not be clear if the block includes synchronization circuits or if a synchronization hazard is present.

Smith describes two separate methods that may be used to model different aspects of synchronization of a signal passing between clock domains. The first method relates to modeling and simulating the behavior of known synchronization elements in the system (in particular as described at column 3, line 66 to column 4, line 42 of Smith.) If a signal arrives at a synchronizer just before the synchronizer is clocked, it may violate the setup and hold times for the first flip-flop in the synchronizer. The signal will therefore not be clocked in at that time and the first flip-flop output will be undetermined. It will therefore require an extra clock cycle for the received bit to be received by the circuit, this variability in timing is often ignored during modeling of the circuit. The method of Smith, provides a model of a synchronizing element that is able to randomly adjust the number of clock cycles required to receive a signal to model this behavior. As described at column 4, lines 36-38 of Smith, the method operates by substituting the model shown in figure 2 for all the synchronizers in the design. This relies on identifying the synchronization elements in the design. There is no disclosure of how the synchronization elements should be identified in Smith.

The second method described by Smith relates to determining whether a signal crossing from one clock domain to another, which is not synchronized, is suitably controlled to ensure that timing violations do not occur. Signals that do not require a synchronizer may occur in the design, for instance when synchronization is assured by controlling the signal with another synchronized signal. The method requires that the original signal be modified such that it exhibits an unknown state for a period of time at least equal to the clock period relative to the period of the receiving clock. If the unknown state is seen to propagate in the system then it is determined that the control of the signal is not adequate to avoid timing violations. However, it is clear that in order to modify the signal, the signal crossing clock domains must be identified.

There is no disclosure of how asynchronous signals that are not received using a synchronizing element are identified in the teaching of Smith.

The applicant submits that Smith does not disclose or suggest the feature of 'determining which if said plurality of functional elements is a synchronizer to thereby identify if there is a synchronization problem for said at least one signal passing from said one clock environment to said another clock environment', as claimed. Furthermore, there is no disclosure or suggestion by Smith of the feature of 'wherein said determining step is arranged to identify if a functional element which is a source of propagation of said unknown state is a hazard or a synchronizer' as recited by claim 1. Rather, for each method described by Smith it is required that all synchronization elements or asynchronous signals crossing clock boundaries must be known. The applicant respectfully submits that Smith does not teach any way of identifying unknown synchronizers or hazards in a circuit design, and nor does it suggest the solution as recited in claim 1. Thus, the applicant submits that claim 1 is novel and non-obvious over Smith.

Independent claim 21 is in accord with claim 1 and is therefore novel and non-obvious for the reasons discussed above. All other claims contained within this application are dependent upon claim 1 and are therefore similarly novel and non-obvious for at least the same reasons.

All claims are therefore believed to be allowable, and all objections are traversed or accommodated.

CONCLUSION

As a result of the foregoing, the Applicant asserts that the remaining Claims in the Application are in condition for allowance, and respectfully requests an early allowance of such Claims.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at ***wmunck@munckbutrus.com***.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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